Design Optimization of Power Electronics Circuits using Genetic Algorithms – A Boost PFC Converter Example

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Abstract — This paper presents an approach to discrete design optimization of a complete power electronics converter with the objective to minimize the total component cost. The design constraints are the converter specifications, such as operating power and voltage ranges, EMI standards, size, and lifetime, as well as the component safe operating areas. The design variables are the switching frequency and the selection of the actual, commercially available components and materials. The genetic algorithm provides for a systematic and efficient search of the databases of preferred components, which contain all (datasheet-based) component parameters that are necessary for evaluating the constraints and the objective function.

The methodology is illustrated with a developed software tool for designing a low-cost boost power factor correction (PFC) front-end converter with an input EMI filter. Computationally fast and experimentally validated algebraic models of the system and its components, which include second order effects, are considered. A graphical user interface for managing the design specifications and the component databases, controlling and monitoring the optimization process, and analyzing the performance of the best designs is described. The results of a design for a 1.15 kW unit are presented.

1. INTRODUCTION

The design of power electronics systems involves a large number of design variables and the application of knowledge from several different engineering fields (electrical, magnetic, thermal, mechanical). In order to simplify the design problem, traditional design procedures fix a subset of the design variables and introduce assumptions (simplifications) based on the designer’s understanding of the problem. These simplifications allow an initial design to be obtained in a reasonable amount of time, but further iterations through hardware prototype testing are usually required. The ability and expertise of the designer usually lead to good but not optimum designs.

Mathematical optimization techniques offer an organized and methodical way of approaching the design problem. This allows the designer to use more design variables and fewer simplifications. This, in turn, reduces the number of iterations during the hardware-testing phase. The increasing speed of computer hardware and the development of faster computational models allow optimum designs to be obtained in a relatively short time. Furthermore, the application of the optimization techniques can provide a better understanding of the trade-offs involved in the design, and even highlight those that were initially ignored.

First attempts at automated computer aided design of power converters coincided with the widespread availability of time-shared computing in the late 1970’s, [1]. Early efforts present a continuous variable optimization approach applied to the design of the power stage of buck, boost, buck-boost and half-bridge dc-dc converters. In [2-4], an optimization algorithm using augmented Lagrangian penalty function is selected to minimize the converter weight, while the passive components, switching frequency and efficiency are considered continuous design variables. Constraints are defined according to the design specifications and physical limitations. Several improvements to this approach were presented in [5] in order to obtain a practical nonlinear optimization tool. In a later paper [6], this tool is used in the design of a boost PFC converter.

Majority of the later efforts concentrate on optimizing a specific component or converter subsystem. In [7], an optimization procedure is used to study the tradeoffs between BJTs and MOSFETs in a half-bridge dc-dc circuit. An optimization procedure for heat sink design is described in [8]. The work on transformer performance optimization [9], led to the development of CAD tool for automated design of magnetic components [10]. In [11], an automated way for cabling design in power electronics converters for the lowest possible inductance, is proposed. Reduced order models are used in [12] to optimize the gate drive circuitry in a half-bridge circuit, while [13] sets a framework for the optimization of the power package design. Some of the studies focused on linking several software packages together and managing them with an optimization program [8, 10, 12, 13] in order to address the multidisciplinary nature of the power electronics design. This method suffers from long simulation times and faces the significant challenge of forcing different software packages to communicate with each other.

Although the above-mentioned studies made a significant impact on the understanding of the power converter design issues and main tradeoffs involved in the design process, most fail to fully capture the discrete nature of the power electronics design. If available discrete components were employed as design variables, much more accurate models (e.g. electrical, magnetic, thermal, mechanical, cost) of each specific component can be used, and the optimization results can be physically realized immediately. Among the discrete optimization methodologies, genetic algorithms (GAs) recently have received attention in power electronics optimization. GAs have been applied to the design of an active filter in [14]. In [15], a buck regulator is designed for optimum transient performance, using GAs. The design

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The current work has been motivated by the need to optimize the design of a complete power electronics product for minimum material cost. As the system components are discrete in nature, the GA approach is selected because it is better suited for obtaining the realistic, globally optimum, system designs. The design variables essentially consist of the databases of commercially available preferred parts, which are augmented with all necessary electromagnetic, thermal, mechanical, reliability, and cost parameters. Because GAs typically require a large number of designs to be evaluated, the steady state algebraic models are used to obtain a computationally efficient method. The component models and parameters are obtained directly from the data sheets, and are experimentally calibrated and modified whenever necessary. The design constraints consist of the product specifications and the component safe-operating-areas as defined in the data sheets.

In the following section, the formulation of the GA for design optimization of the power electronics circuits is presented. In Section III, the optimization problem is defined on an example of a specific power electronics product consisting of the single-ended boost power factor correction (PFC) converter and EMI filter. In Section IV, the software tool developed to perform the optimization process is described while in Section V, a design of a 1.15 kW unit, using the proposed methodology, is presented.

II. GA-BASED OPTIMIZATION ALGORITHM

GAs (conceived by Holland [19]) are probability-based algorithms that utilize the processes of natural selection, and have been experimentally proven to be robust in their application to many search problems [20]. A population of individuals is used to simulate the breeding environment, with each individual representing a single design that is coded using a gene string. GAs are ideal for discrete design problems because each gene is restricted to a pre-defined set of values, with one or more genes typically representing a single variable in the design problem. For a converter design, each string is used to represent a set of components that define one possible converter design. To implement this approach, a database of possible choices for each component must be created. Each gene in the string is then used as an index to a specific component in its corresponding database. For example, consider a simplified power converter that is comprised of a switch, inductor, and capacitor. Next, assume that each component in the system may be selected from its corresponding database shown in Table I. For this configuration, a 3-gene genetic string could be used to represent the power electronics system (one gene for each component), with each gene in the string having its own alphabet of index values, as shown in Fig. 1.

### Table I. COMPONENT DATABASES FOR A SAMPLE POWER CONVERTER.

<table>
<thead>
<tr>
<th>Index</th>
<th>Switch (first gene)</th>
<th>Core (second gene)</th>
<th>Capacitor (third gene)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IRG4B430W</td>
<td>T157-26</td>
<td>ECE-S2GU680J</td>
</tr>
<tr>
<td>2</td>
<td>IRG4B430W</td>
<td>T200-40B</td>
<td>ECO-S2GP680BA</td>
</tr>
<tr>
<td>3</td>
<td>HGTG20N603B3D</td>
<td>58906-A2</td>
<td>ECO-S2GP2210A</td>
</tr>
<tr>
<td>4</td>
<td>IRFP22N50A</td>
<td></td>
<td>ECE-S2WU331Z</td>
</tr>
<tr>
<td>5</td>
<td>IXH21N30</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Alphabet Definitions:**
- gene 1: (1, 2, 3, 4, 5)
- gene 2: (1, 2, 3)
- gene 3: (1, 2, 3, 4)

**Sample Genetic String:**
- gene 1 gene 2 gene 3:
  - 4 2 1

**Actual Design:**
- IRFP22N50A
- T200-40B
- ECE-S2GU680J

Fig. 1. Gene string representation of a sample power converter.

The GA procedure is initialized by randomly creating a population of designs. The characteristics of each design are used to generate a fitness value (dependent on the cost with appended constraints) indicating its level of performance with respect to the other designs in the population. Designs that perform the best are given the greatest probability of breeding with other good designs so that their characteristics can be passed to future generations. For example, the highest fitness values would be assigned to those designs with the lowest cost that do not violate the maximum operating temperature of any of the components.

Breeding is carried out by applying various genetic operators that systematically recombine selected parent strings from the current population to form child strings that will hopefully yield characteristics with better performance than their predecessors. Each genetic operator is applied with a specific probability that may be adjusted to improve the efficiency of the genetic algorithm. The genetic operators that have been used in our case are the crossover and mutation. They are illustrated in Fig. 2 using the sample 3-component system described above.

**Parent 1:**

- 4 2 1

**Before Mutation:**

- 5 2 2

**Mutation Point:**

- 5 1 2

**Child 1:**

- 5 2 2

**After Mutation:**

- 5 1 2

**Child 2:**

- 4 3 1

Fig. 2. Genetic operator procedures: (a) crossover, (b) mutation.

A uniform crossover procedure is implemented by drawing a uniformly distributed random number for each gene in the string. If the random number is less than or equal to 0.5, then the gene from the first parent is passed on to the first child and the gene from the second parent is passed on to the second child. The procedure is reversed if the ran-
dom number is greater than 0.5. Crossover is the GA’s primary means of interrogating the design space and, thus, is applied with a high probability between 0.7 and 1.0, which means in almost every generation.

The mutation operator is implemented by generating a uniformly distributed random number to identify which gene in the string will change its value. For a 3-gene string, a random number in [0, 0.33) would apply mutation to the first gene, the number in [0.33, 0.66) would apply mutation to the second gene, and so on. After a gene has been identified for mutation, another random number is generated to determine its new value from the list of choices in the alphabet. The mutation operator provides a random search capability, which may discover new areas of the design space with information that can improve a design’s performance, and thus increases the probability of finding the global optimum. Mutation is typically applied with a small probability between 0.001 and 0.05, so that it does not prevent the GA from converging.

After the child designs have been created, an elitist selection scheme is often implemented to form the next generation. It involves replacing the worst design in the child population with the best design in parent population to ensure that the best design is always preserved. One population after another is created until a convergence criterion is satisfied.

In addition to discrete variables, the optimizer also has the capability of handling a small number of continuous variables. Specialized genetic operators are used to manipulate the continuous variable values from each parent design to produce a new value for the resulting child design. This feature is used to design the switching frequency and the inductor number of wire-turns.

III. DEFINITION OF THE OPTIMIZATION PROBLEM

In this section, the proposed optimization approach will be formulated on an example of a low-cost boost PFC front-end converter with input EMI filter. The same design problem was treated in [22] using a continuous variable optimization approach, with the objective to acquire a better understanding of the system behavior and main trade-offs.

A. System Specifications and Fixed Design Variables

The system to be designed consists of the boost PFC converter with an EMI filter, as shown in Fig. 3. The design specifications include: output power \( P_o \), input voltage range \( (V_{in_{min}}, V_{in_{nom}}, V_{in_{max}}) \), line frequency, maximum value of the output voltage \( V_{o_{max}} \), ambient temperature, and maximum temperature of the heat sink (HS). The design must also meet the corresponding PFC [23] and EMI [24] standards.

The controller components are not included in the design optimization, but are selected to provide constant-frequency average-current-mode control for continuous-current-mode operation as described in [25]. Based on the load requirements, the output capacitor, \( C_b \), and the average value of the output voltage, \( V_o \), are determined independently considering \( V_{o_{max}} \), the maximum peak value of the input voltage, and controller tolerances.

![Fig. 3. EMI filter and boost PFC stage schematic.](image)

The complete design of the boost inductor \( L_b \) is included, but only toroidal cores are considered since this appeared to be the more cost-effective for this application. The common mode choke design is limited to the selection of commercially available complete components.

A final simplification is made by assuming the layout to be fixed. The component and layout parasitic capacitances and inductances were estimated and experimentally calibrated for a given layout and component choice, and were not changed throughout the design process.

B. Design Variables

The remaining variables of the system, listed in Table II, constitute the set of design variables.

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Design Variable</th>
<th>Type</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMI Filter</td>
<td>Common mode Choke (L_CM)</td>
<td>discrete</td>
<td>AUC^8</td>
</tr>
<tr>
<td></td>
<td>Differential mode capacitor (C_CM)</td>
<td>discrete</td>
<td>2· AUC</td>
</tr>
<tr>
<td></td>
<td>Common mode capacitor (C_0)</td>
<td>discrete</td>
<td>2· AUC</td>
</tr>
<tr>
<td>Boost Inductor (L_b)</td>
<td>Core</td>
<td>discrete</td>
<td>AUC</td>
</tr>
<tr>
<td></td>
<td>Wire</td>
<td>discrete</td>
<td>( n\cdot\text{MLT-AUC}_{wire} + )</td>
</tr>
<tr>
<td>Semi-conductor Devices</td>
<td>Number of turns</td>
<td>continuous ((n))</td>
<td>AUC</td>
</tr>
<tr>
<td></td>
<td>Active switch ((S))</td>
<td>discrete</td>
<td>AUC</td>
</tr>
<tr>
<td></td>
<td>Switching frequency</td>
<td>continuous</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>Rectifier diode ((D_r))</td>
<td>discrete</td>
<td>4· AUC</td>
</tr>
<tr>
<td></td>
<td>Fast diode ((D_f))</td>
<td>discrete</td>
<td>AUC</td>
</tr>
<tr>
<td>Thermal Management</td>
<td>Heat sink (HS) (\theta_{ca})</td>
<td>continuous ((R_{ca}))</td>
<td>( k_s/R_{ca} )</td>
</tr>
</tbody>
</table>

V: Actual Unit Cost from a database of commercial components.

Most of the design variables are discrete circuit components described by a set of parameters. For instance, a boost inductor wire is defined by assigning values to its four defining parameters for each wire-type, namely: diameter, copper cross-section area, maximum temperature, and cost per unit length (AUC_{wire}). The switching frequency is a continuous variable and is treated as such in the optimization code using specialized continuous variable operators. The number of turns is an integer and, hence, discrete, but due to the large number of possible values, it is more efficient to treat it also as continuous variable. Although the heat sinks (and possibly fans) are discrete components and should be treated as such, out of necessity we used the thermal resistance from the device case to the ambient as a substitute variable, because our database of these components was inadequate.
C. Objective Function

The objective function is the actual cost of all the components of the circuit shown in Fig. 3. Hence, the optimization goal is to obtain a set of components from Table II that minimizes this function. Each of the components in a database contains a parameter specifying its actual unit cost (AUC). As shown in Table II, the cost of the boost inductor windings is calculated as the sum of the wire cost and the assembly cost, which was assumed proportional to the number of turns. The heat sink cost was assumed inversely proportional to the thermal resistance. The coefficients for the winding and heat sink costs, \( k_w \) and \( k_h \), were approximated from a limited set of available commercial components.

D. Constraints

The design variable choices that minimize the objective function must be found subject to several constraints defined according to the design specifications, physical limitations, and component safe operating areas. These constraints are specified below.

Design Specifications

1. Continuous current mode: The maximum peak-to-peak current ripple in the boost inductor cannot be higher than 150 % of the average peak inductor current.
2. EMI: The harmonics around the lowest multiple of the switching frequency within the EMI standard must be below the standard by 3 dBμV.
3. Surface temperatures of all components must be below a specified maximum value.

Physical limitations

4. The boost inductor winding must fit in the available window area of the core.

Component Safe Operating Areas

5. The peak value of the flux density in the boost inductor core cannot exceed the material saturation flux density.
6. The voltage ratings of all devices must be larger by a certain margin than the maximum voltages on them.
7. The peak current ratings of all diodes must be larger than the pre-calculated inrush current.
8. The current ratings of the EMI filter components must be larger than the maximum rms current through them.
9. The junction temperatures of all semiconductor devices must be below 125°C.
10. The boost inductor core temperature must be below the value corresponding to a desired core lifetime.

Upper and lower boundaries on the continuous variables can be specified by user. The PFC standard [23] is always satisfied with this topology, so it was not considered.

E. Models and Assumptions

For computing the value of the various constraints as a function of the design variables, numerous models and assumptions were applied. [22]. In order to reduce the computation time, only the steady state algebraic models are used. Whenever available, the detailed steady state algebraic models from the data sheets and application notes of the component manufacturers are utilized. The parameter tolerances also are considered when available, and can be taken into account to a user-specified degree.

It is important to note that the boost inductor wire and core are not selected based on the maximum rms current and peak ampere-turns, but based on the maximum boost inductor temperature. This required modeling of the second order effects such as the saturation of the boost inductor core as a function of the dc magnetizing force, ac flux density, core temperature, and switching frequency. The skin and proximity effects are considered in the calculation of the winding losses. At the end, the final models for boost inductor temperature-rise had to be experimentally calibrated.

The nominal current ratings of the semiconductor devices also are not explicitly considered, but instead the junction and case temperatures are limited. This required detailed modeling of the conduction and switching losses for all devices, including the fast diode reverse recovery losses, the switching losses due to overlap of the voltage and current, and the losses due to the parasitic interconnect series inductance. Because the thermal models for the EMI filter components were not available, their selection is based on the rms current ratings.

The methodology for modeling of the EMI follows the analytical approach presented in [26]. The simplified noise-source models consist of the boost inductor current for the differential mode (DM), and of the voltage between the switch collector (or drain) and the ground, for the common mode (CM). The ringing in the voltage across the switch and diode was neglected. The propagation path models include the parasitic capacitances and inductances of all the components in Fig. 3, of the circuit layout, and of the line impedance stabilization network (LISN). The values of most of the parasitics were estimated, and only several critical ones were calculated and calibrated with experiments. The CM choke leakage inductance (functioning as DM filter inductance) is estimated at 3%, and the boost inductor inductance is approximated with its average value over the line cycle. Due to the approximate nature of the employed EMI models, their validity is expected and was experimentally verified only in the low frequency range (below few megahertz).

The computationally efficient and sufficiently accurate modeling of the thermal and EMI phenomena presented a significant challenge. This required detailed experimental study of different designs [27] and the calibration of the models on several prototypes using different combinations
of component designs and operating at different conditions. Table III illustrates the obtained level of agreement between the experimental and predicted results (considering component tolerances) after model calibration.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Predicted</th>
<th>Experimental</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_r$ rms (A)</td>
<td>4.32</td>
<td>4.40</td>
</tr>
<tr>
<td>$I_{\text{rms}}$ (A)</td>
<td>7.0</td>
<td>7.8</td>
</tr>
<tr>
<td>$I_{\text{max}}$ (A)</td>
<td>1.8</td>
<td>3.4</td>
</tr>
<tr>
<td>$T_c$ (µH)</td>
<td>656</td>
<td>1204</td>
</tr>
<tr>
<td>$T_{\text{sat}}$ (ºC)</td>
<td>131</td>
<td>156</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (S)</td>
<td>61.6</td>
<td>63.1</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (DF)</td>
<td>41.8</td>
<td>41.8</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (DR)</td>
<td>94.1</td>
<td>94.8</td>
</tr>
<tr>
<td>$I_{\text{in}}$, rms (A)</td>
<td>4.36</td>
<td>4.40</td>
</tr>
<tr>
<td>$I_{\text{peak}}$ (A)</td>
<td>7.0</td>
<td>7.6</td>
</tr>
<tr>
<td>$\Delta I_{\text{max}}$ (A)</td>
<td>3.4</td>
<td>3.2</td>
</tr>
<tr>
<td>$L_c$ min (µH)</td>
<td>656</td>
<td>1204</td>
</tr>
<tr>
<td>$T_{\text{core}}$ (LB)</td>
<td>131</td>
<td>156</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (S)</td>
<td>61.6</td>
<td>63.1</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (DF)</td>
<td>41.8</td>
<td>41.8</td>
</tr>
<tr>
<td>$T_{\text{case}}$ (DR)</td>
<td>94.1</td>
<td>94.8</td>
</tr>
<tr>
<td>Critical EMI level $^*$</td>
<td>49.3</td>
<td>58.5</td>
</tr>
<tr>
<td>DM (dBµV)</td>
<td>48.5</td>
<td>57.7</td>
</tr>
<tr>
<td>CM (dBµV)</td>
<td>41.6</td>
<td>50.7</td>
</tr>
<tr>
<td>Total (dBµV)</td>
<td>49.3</td>
<td>58.5</td>
</tr>
</tbody>
</table>

V: Tambient = 30 ºC $^*$: At full power and nominal voltage

IV. SOFTWARE TOOL

A software tool called OPES has been developed to encapsulate the approach described in the previous sections. The GA optimizer, DARWIN [21], and the steady-state algebraic design analysis were coded in FORTRAN. The graphical user interface was created in JAVA. The main features of the software tool are described below.

A. Control and Monitoring of the Optimization Process

The optimization process is controlled and monitored from the main window shown in Fig. 4. Another window, which allows entering the design specifications and conditions, can be accessed from here. These conditions contain a wide variety of parameters such as the output power level, input and output voltages, and the values of the different layout parasitics according to the selected layout. The user can also select the EMI standard to be considered, whether a single heat sink for all devices or separated heat sinks should be used, and how conservative the design analysis results should be. The optimization process population size and the number of generations can be specified in the main window. A specified number of the best designs found by the optimizer can be displayed at any time during the optimization process. The percentage of the optimization process completed is also displayed.

B. Component Databases

The software tool also allows the user to manage the component databases that are used in the optimization process. Component databases for the EMI filter capacitors, CM choke, switch (IGBT and MOSFET), fast diodes, bridge diodes, cores and wires have been created. The user can update and organize these databases as required, using the windows like the one shown in Fig. 5.

C. Design Reports

After the optimization process has completed, a report can be generated detailing each of the best designs found. This design report includes a detailed cost break-down of the design, status of the different constraints, electrical performance information (general and specific for each component), and a set of plots containing information on the EMI levels, boost inductor current waveform envelope, boost capacitor voltage, and duty-ratio. Fig. 6 shows some of the windows containing this information.
V. DESIGN STUDY EXAMPLE

The software tool described above was used to design a 1.15 kW unit and a prototype was built. This prototype is shown in Fig. 7 together with the design specifications. A cost reduction of approximately 15% was reached compared to a previous design obtained following a traditional design methodology, where a choice of switching frequency and boost inductance was left to the designer’s intuitive understanding of the problem.

![Fig. 7. Specifications and optimum design prototype.](image)

VI. CONCLUSIONS

The presented GA-based design approach to optimization of power electronics circuits is shown to be a very effective and powerful tool for obtaining improved solutions compared to traditional design procedures. Future design tools based on this approach could also be used to rapidly provide an estimation of the minimum cost of the system under certain design specifications and conditions, and to vary the specifications and operating conditions in order to investigate possible ways of reducing the system cost, etc. Due to the short time required to obtain this information, the tool is therefore also especially useful for initial project evaluations (viability, etc.) and for the design of different products within one platform.

The widespread application of the proposed approach critically hinges on the availability and future development of better component and system loss, thermal, EMI, and reliability models.

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REFERENCES


