Abstract — This paper presents inverter control strategies to compensate for the distorting effects of unbalanced and non-linear loads in 4-leg inverter-fed power systems. Synchronous frame controllers are utilized at selected frequencies to eliminate positive and negative sequence distortion. Additionally, stationary frame controllers are employed to attenuate zero sequence distortion due to non-zero neutral currents. Combined with fundamental control this strategy is demonstrated to achieve a high level of performance under challenging loading conditions.

I. INTRODUCTION

The problem of unbalanced and distorted voltages in power systems is not a new one. It has been understood for several decades that such conditions can cause malfunction of or even damage to power consuming and power processing equipment. With the ever-increasing use of electronic equipment, this issue is becoming more prevalent, as electronic loads often cause and are sensitive to unbalanced and distorted voltages.

In light of the numerous applications for high power, high performance, three-phase voltage source inverters (VSIs) in the modern world, and the difficulties involved in their design, it is the objective of this paper to present advanced control strategies for increased inverter performance under challenging loading conditions. Presently, extra hardware (either passive or active) is usually employed in order to produce acceptable power waveforms from high power inverters [1]. However, additional circuitry is bulky, expensive, and lossy. Therefore, recent research has centered on unconventional control techniques to increase inverter performance under unbalanced and non-linear loading [1]-[8].

The concepts of synchronous frame control for unbalanced load compensation and non-linear load compensation are presented in [2] and [3], respectively. A fourth leg is often added to VSIs, as depicted in Fig. 1, in order to enable the control of zero sequence distortion in the power system. However, low switching frequencies limit the voltage control bandwidth, and likewise limit the effectiveness of adding a fourth VSI phase leg to attenuate zero sequence distortion through conventional control techniques. While synchronous frame controllers are effective in both three-leg and four-leg VSIs for controlling negative and positive sequence distortion, they cannot be applied to address the problem of zero sequence distortion in four-leg VSIs. This paper presents a technique based on the transformation of integral synchronous frame controllers into the stationary frame [4], [5] to achieve near zero steady state errors for the zero sequence distortion created by unbalanced and specific non-linear loads.

Because of the limited voltage control bandwidth in high power, three-phase VSIs, the difficulties of controlling voltage harmonics become even more pronounced in systems with high output fundamental frequencies. Simulation results for the proposed control techniques will be presented for a high fundamental output frequency, four-leg VSI.

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II. SYNCHRONOUS FRAME CONTROLLERS

Synchronous frame control is often employed in order to achieve zero steady state errors for the fundamental, positive sequence component of the output. A rotating reference frame is utilized, such that the fundamental, positive sequence components of the time-varying abc-voltages become DC quantities in the dqo-coordinate system. This is accomplished through the well-known Park’s Transformation, which is displayed in the Appendix.

Fig. 2 displays a block diagram of synchronous frame control for fundamental, positive sequence compensation. The line to neutral output voltages, $V_{a,b,c}$, are compared to the references, $R_{a,b,c}$, yielding the abc-coordinate error signals, $E_{a,b,c}$. These can be transformed into a reference frame rotating in the positive sequence (CCW direction in the stationary frame) at the fundamental frequency, $\omega$, to obtain the dqo error signals, $E_{d,q,o}$. Integral compensation in this rotating reference frame will result in the DC component of the dqo error signals being driven to zero, and likewise, zero steady state errors will be achieved for the fundamental, positive sequence component of the output. The commanded dqo duty cycles, $D_{d,q,o}$, are input to a 3-dimensional Space Vector Modulation (SVM) scheme [1] in order to select the appropriate gate signal vector, $G_{a,b,c,o}$.

A) Synchronous Frame Control for Unbalanced Loads

In three-phase, three-wire systems (delta connected sources and loads), unbalanced loads create negative sequence currents, and likewise, negative sequence voltage distortion. An unconventional control technique has been proposed in [2] to compensate for the negative sequence voltage distortion due to unbalanced loads in three-phase, three-wire systems. Reference [2] proposes the construction of a synchronous reference frame rotating at the fundamental frequency in the opposite direction as the positive sequence. Thus, the negative sequence, fundamental components of the output voltage will become DC quantities in this negative sequence dq reference frame. With a parallel controller in the negative sequence dq reference frame, the negative sequence distortion can be attenuated, or even eliminated if an integral controller is used. Reference [2] has demonstrated this concept in simulation and experimentation, with the predicted results.

B) Synchronous Frame Control for Non-Linear Loads

Diode rectifiers (both single-phase and three-phase) draw currents at the $\left[(6 \cdot n)\pm 1\right] \cdot \omega$ harmonic frequencies, where $n$ is any positive, real integer. All of the $\left[(6 \cdot n)\pm 1\right] \cdot \omega$ currents exist in the positive sequence, and all $\left[(6 \cdot n)\pm 1\right] \cdot \omega$ currents exist in the negative sequence.

III. STATIONARY FRAME CONTROLLERS

The result of the harmonic currents flowing through the finite output impedance of the VSI is distortion at these harmonic frequencies. A similar control technique to that demonstrated for unbalance control [2] has been proposed for the control of harmonic frequencies [3]. By rotating the output voltage error signals into dq reference frames rotating at the harmonic frequencies, those harmonic disturbances become DC quantities. For example, the negative sequence distortion at the 5th harmonic frequency becomes a DC magnitude in the dq reference frame rotating at $5 \cdot \omega$ in the negative (CW) direction. The error signal in each of the rotating harmonic frames can then be integrated and the result added into the dq-channel duty cycles in the fundamental reference frame, in order to achieve zero steady state errors for the compensated harmonics. This concept has been validated through simulation and experimentation for a three-phase, three-wire VSI in [3].
\[ G_{y}(s) = \frac{2K_i \cdot s}{s^2 + \omega_r^2} \]  

(2)

It is clear in (2) that there is infinite gain at the bandpass filter resonant frequency, \( \omega_r \). Using this knowledge, it is proposed here that zero-damping bandpass filters can be used in the stationary o-channel controller in order to eliminate the zero sequence distortion in three-phase, four-leg VSI.

**A) Stationary Frame Control for Unbalanced Loads**

In three-phase, four-wire systems, unbalanced loads create zero sequence distortion at the fundamental frequency. By placing a parallel path in the o-channel controller, containing a zero-damping bandpass filter with a resonant frequency of \( \omega_r \), the loop gain will be infinite at the zero sequence disturbance frequency. This will make zero steady state errors possible for the zero sequence distortion from unbalanced loads. Fig. 3 displays a block diagram of the zero sequence controller described above included with the fundamental synchronous frame controller.

**B) Stationary Frame Control for Non-Linear Loads**

Single-phase diode rectifiers cause zero sequence distortion at the odd triplen harmonics (3\(^{rd}\), 9\(^{th}\), etc.) in three-phase, four-wire systems. This distortion exists as disturbances in the stationary o-channel at the same harmonic frequencies, and thus cannot be rotated into a reference frame to be represented as DC quantities. For this reason, zero damping bandpass filters, as described above, can be utilized to increase the loop gain to approach infinity at the harmonic frequencies of interest. With an infinite loop gain at the odd triplen harmonics, zero steady state errors can be achieved for these frequencies. A controller to eliminate a zero sequence harmonic disturbance due to single-phase diode rectifiers would take the same structure as that depicted in Fig. 3; however, the zero-damping bandpass filter would be centered at the harmonic frequency of interest. If more than one of the odd triplen harmonics were to be compensated for, additional bandpass filters at those frequencies would be placed in parallel with the one shown in Fig. 3.

**IV. PROPOSED CONTROL STRUCTURE**

By combining the strategies of the previously demonstrated synchronous frame control with the proposed zero sequence control, inverter performance can be greatly increased under challenging unbalanced and non-linear loading conditions.

**A) Proposed Control Structure for Unbalanced Loads**

Because unbalanced loads create both negative and zero sequence distortion in three-phase, four-wire systems, the VSI control structure must contain three distinct controllers in order to produce a purely fundamental output:

1) a positive sequence, synchronous frame integral controller rotating at the fundamental output frequency to ensure perfect tracking of the positive sequence component of the reference,
2) a negative sequence, synchronous frame integral controller rotating at the fundamental output frequency to eliminate the negative sequence distortion created by unbalanced loads, and
3) a zero sequence, stationary frame controller with infinite gain at the fundamental output frequency to eliminate the zero sequence distortion created by unbalanced loads.

Fig. 4 displays a block diagram of this proposed control structure.

**B) Proposed Control Structure for Non-Linear Loads**

Considering single-phase and three-phase diode rectifier loads, the VSI control structure will require three categories of controllers for purely fundamental output performance:

1) a positive sequence, synchronous frame integral controller rotating at the fundamental output frequency to ensure good tracking of the positive sequence component of the reference,
2) positive and negative sequence, synchronous frame integral controllers corresponding to the odd triplen harmonic frequencies created by the diode rectifiers, and
3) zero sequence, stationary frame controllers with infinite gain at the odd, triplen harmonic frequencies to eliminate the zero sequence distortion created by diode rectifiers.

It is clear that to truly achieve zero steady state errors for non-linear loads, an infinite number of integral harmonic controllers would be required, because diode rectifiers draw currents at an infinite number of harmonic frequencies. Despite the impossibility of true zero steady state error operation, a significant improvement in VSI performance can be realized by simply compensating for the dominant low-order harmonics.

Because of the significant phase lag at harmonic frequencies due to system delays, a leading angle must be added for each of the harmonic controllers. As proposed in [3], this can be accomplished for the synchronous frame.
controllers by simply adding a leading angle, \( \Phi_k \), into the inverse Park's Transformation, as displayed in the Appendix. However, the stationary frame controllers do not undergo a rotation in the change of basis, so this simple solution does not apply. Thus, a phase lead transfer function will be required in the forward path of each of the zero sequence controllers, in order to compensate for the phase lag.

Fig. 5 displays a block diagram of the proposed control structure for non-linear load compensation.

V. SIMULATION RESULTS

In order to demonstrate the merit of the control strategies discussed above, the results of SABER simulations are presented below. The nominal output parameters for the simulations are presented in Table I.

A) Results for Unbalanced Load

The unbalance phase loading simulated and used in this paper is: phase a and phase b at full nominal load and phase c at no-load. This is a severe unbalance that is unlikely in practice; however, it effectively demonstrates the merit of the proposed control structure. Fig. 6 displays the output phase voltages under this unbalanced load with a low voltage bandwidth controller of the structure depicted in Fig. 2. A horizontal line is provided to show the nominal peak voltage of \( 115 \cdot \sqrt{2} \) V. Under this case, the fundamental controller alone cannot compensate for the negative and zero sequence distortion caused by the load. Consequently, the output is severely unbalanced with a maximum phase unbalance of 45% from nominal.

Using the three-sequence control structure of Fig. 4, the negative and zero sequence distortion is significantly attenuated, resulting in the output phase voltages displayed in Fig. 7. The maximum phase unbalance is reduced to 1.2% from nominal. Zero steady state errors are not truly achieved, because some damping was added to the zero sequence bandpass filter for implementation.

<table>
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<th>TABLE I</th>
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<tr>
<td>NOMINAL VSI OUTPUT PARAMETERS</td>
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<tr>
<td>( V_{\text{out},l-n} )</td>
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<tr>
<td>( f_{\text{out}} )</td>
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<tr>
<td>( P_{\text{out}} )</td>
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B) Results for Non-Linear Load

Two separate non-linear loads were simulated for the purposes of this paper: a three-phase diode rectifier and a balanced load of single-phase (line to neutral) diode rectifiers. For both load cases, a total output power level of 90 kVA was simulated. It is unlikely in practical implementation for the full nominal load to consist only of non-linear loading; however, this severe loading case serves to prove the proposed control concept. Fig. 8 and Fig. 10 display the output phase voltage in the time and frequency domain with only a low bandwidth voltage controller for the three-phase diode rectifier load and the balanced load of single-phase diode rectifiers, respectively. Under the three-phase diode rectifier load, the output phase voltage has a THD of 22.1% with the dominant harmonics being the 5th and 7th. The load of single-phase diode rectifiers results in an output THD of 11.4% with the 3rd, 5th, and 7th being the dominant harmonics.

Using the control structure of Fig. 5, with negative sequence 5th harmonic and positive sequence 7th harmonic controllers activated, the THD for the three-phase diode rectifier load is reduced to 3.8%, as shown in Fig. 9. It is clear from the frequency domain plot that near zero steady state errors are achieved for 5th and 7th harmonic component of the output. Adding the zero sequence 3rd harmonic for the
load of single-phase diode rectifiers results in an output THD of 2.1%, as displayed in Fig. 11. Again, near zero steady state errors are achieved for the 5th and 7th harmonic; however, the 3rd harmonic is only attenuated by approximately 15 dB because of the damping added to the bandpass filter for practical implementation.

Fig. 6. Output phase voltages under severe unbalanced load with fundamental controller alone

Fig. 7. Output phase voltages under severe unbalanced load with proposed control structure

Fig. 8. Output phase voltage in the time and frequency domain under three-phase diode rectifier load with fundamental controller alone

Fig. 9. Output phase voltage in the time and frequency domain under three-phase diode rectifier load with proposed control structure

Fig. 10. Output phase voltage in the time and frequency domain for load of single-phase diode rectifiers with fundamental controller alone

Fig. 11. Output phase voltage in the time and frequency domain for load of single-phase diode rectifiers with proposed control structure
VI. CONCLUSION

Previous research [2], [3] has demonstrated the merits of synchronous frame controllers in three-phase, three-leg inverters. While this strategy is easily extended to three-phase, four-leg inverters, stationary frame controllers, as proposed in this paper, are required to attenuate zero sequence distortion. Combining these two strategies, a control structure has been developed in this paper that has been demonstrated through simulation to significantly enhance inverter performance under challenging loading conditions.

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REFERENCES


APPENDIX

Shown below is Park’s Transformation to change basis from abc-coordinates to dqo-coordinates.

$$T_{abc \rightarrow dqo} = \begin{bmatrix} \frac{2}{\sqrt{3}} & -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

Shown below is the inverse Park’s Transformation, including a leading angle, $\phi_k$, for the harmonic number, $k$.

$$T_{dqo \rightarrow abc} = \begin{bmatrix} \cos(\omega t + \phi_k) & -\sin(\omega t + \phi_k) & 1 \\ \cos\left(\omega t - \frac{2\pi}{3} + \phi_k\right) & -\sin\left(\omega t - \frac{2\pi}{3} + \phi_k\right) & \frac{1}{\sqrt{3}} \\ \cos\left(\omega t - \frac{2\pi}{3} + \phi_k\right) & -\sin\left(\omega t - \frac{2\pi}{3} + \phi_k\right) & \frac{1}{\sqrt{3}} \end{bmatrix}$$